

WEST[Help](#)[Logout](#)[Interrupt](#)[Main Menu](#) [Search Form](#) [Posting Counts](#) [Show S Numbers](#) [Edit S Numbers](#) [Preferences](#)**Search Results -**

Terms	Documents
-----------------------	---------------------------

15 near4 17	13
-------------	----

Database:

15 near4 17

Search History

Today's Date: 3/29/2001

<u>DB Name</u>	<u>Query</u>	<u>Hit Count</u>	<u>Set Name</u>
USPT	15 near4 17	13	<u>L9</u>
USPT	17 same l2	0	<u>L8</u>
USPT	test adj1 clip	212	<u>L7</u>
USPT	15 near4 11	25	<u>L6</u>
USPT	plurality	1240968	<u>L5</u>
USPT	11 and l2	8	<u>L4</u>
USPT	11 same l2	0	<u>L3</u>
USPT	system adj1 operation	30795	<u>L2</u>
USPT	probe adj1 line	349	<u>L1</u>

WEST

 Generate Collection

L6: Entry 19 of 25

File: USPT

Apr 27, 1993

DOCUMENT-IDENTIFIER: US 5206862 A

TITLE: Method and apparatus for locally deriving test signals from previous response signals

DEPR:

FIG. 1 shows local test circuitry 10 residing on an integrated circuit 12 to be tested. The test circuitry 10 includes a test point array 14, a plurality 15 of probe line drivers 16, a plurality 17 of control/sense line drivers/receivers 18, 19, an instruction register 20, a data register 22, a multiplexor 24, and demultiplexors 26, 28. The IC 12 includes external pin contacts for receiving a test clock signal TCK, a test enable signal TE, a test input signal TI and a test output signal TO. The function of the test circuitry 10 is to generate control signals (e.g., test signals) for select test points of the test point array 14, while monitoring resulting response signals.

CLPR:

1. A method for defining a test signal for an IC test point based upon a logic state of a signal path local to the IC, the IC having an integral test structure comprising a plurality of probe lines, a plurality of control/sense lines and a data register, said data register for storing a first data pattern, the method comprising the steps of:

CLPR:

6. A method for defining a test signal for an IC test point based upon a logic state of a signal path local to the IC, the IC having an integral test structure comprising a plurality of probe lines, a plurality of control/sense lines and a data register, said data register for storing a first data pattern, the method comprising the steps of:

CLPR:

7. An apparatus for defining a test signal for an IC test point based upon a logic state of a signal path local to the IC, the IC having an integral test structure comprising a plurality of probe lines, a plurality of control/sense lines and a data register, said data register for storing a first data pattern, the apparatus comprising: